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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,838	TAKATA, YUKARI	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/23/03, 8/26/05 and 11/14/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

2. Acknowledgement of papers filed: application on 7/23/2003, status requests on 8/26/2005 and 11/14/2005. The papers filed have been placed on record.

Priority

3. Receipt of papers submitted under 35 U.S.C. 119(a)-(d) is acknowledged; the papers have been placed on record in the file. The certified copy of 2002-216769, filed on 07/25/2002 has been received and placed on record.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

6. Claims 17-18 are objected to because of the following informalities: grammatical errors. Claim 17 calls for "said first process including *a process that* said instruction execution stage executing..." and "said second process including

a process that said instruction stage executing...". The limitations include improper English grammar, appropriate correction is required.

7. Furthermore, claim 17 states, "said instruction stage executing interrupt instruction" (lines 19-20), however, there is no previously claimed "instruction stage", thus the limitation lacks antecedent basis. Examiner will interpret the limitation as, "said instruction *execution* stage executing interrupt instruction" for the remainder of the examination.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 16 and 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. As per claim 16, the limitation "said interrupt instruction" lacks antecedent basis. The intention of the limitation is unclear, as it could be interpreted as "said interrupt request", a new, previously unmentioned "interrupt instruction," or another interpretation. Therefore, for the remainder of the application the limitation, "said interrupt instruction" will be interpreted as "said interrupt request".

11. As per claim 19, the limitation, "said first burst transfer is suspended and a second program as a branch target is executed." It is unclear what "*a second*

program as a branch target is executed" means and therefore the metes and bounds of the limitation are unknown.

12. As per claim 20, the limitation, "said second burst transfer is suspended and a third program as a branch target is executed." It is unclear what "*a second program as a branch target is executed"* means and therefore the metes and bounds of the limitation are unknown.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

14. Claims 1-4, 7 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Moyer, U.S. Patent 6,775,727.

15. As per claim 1, Moyer teaches a data processor comprising:

a. A processor: [CPU 14, fig. 1.]

b. A first storage device: [System Memory(s) 20, 22 and/or 24, fig. 3.]

c. And a second storage device connected between said processor and said first storage device: [Cache 18, fig. 3.]

d. Wherein when a predetermined data required by said processor does not exist in said second storage device, a plurality of data corresponding to one line of said second storage device, including said predetermined data are read from said first storage device and transferred to a certain line of said second storage device by burst transfer: [Col. 3, lines 10-53.]

e. Whereby when an interrupt request occurs during said burst transfer, said burst transfer is suspended and an interrupt processing is started: [Figs. 5 & 6, col. 6, lines 46-55, and more specifically explained on col. 6, line 56 to col. 7, line 36. The control bits are set to allow interrupts to occur on burst transfers, including when the cache is reading data from memory.]

16. As per claim 2, Moyer teaches the data processor according to claim 1 wherein said burst transfer suspended is restarted after the completion of said interrupt processing. [When a high priority interrupt occurs and halts the cache burst transfer, it is later resumed. Col. 6, lines 46-55. It is inherent that the interrupt processing is complete, since the original burst is resumed and the bus cannot perform the interrupt processing and original burst processing at the same time.]

17. As per claim 3, Moyer teaches the data processor according to claim 2 wherein said burst transfer suspended is restarted only when returning to the

original program in which said burst transfer is suspended. [The burst transfer is a component of an inherent program that causes it to occur, therefore, when the burst transfer resumes, the program has also been returned too.]

18. As per claim 4, Moyer teaches the data processor according to claim 2 wherein when a plurality of interrupt requests occur a plurality of interrupt processing are executed sequentially and, after the completion of the burst interrupt processing, said burst transfer suspended is restarted: [When a plurality of interrupt requests are received that meet the criteria set out by the control field encodings (shown in figs. 5 & 6), the burst transfer will be interrupted a plurality of times. The burst transfer will then be resumed after the interrupt is handled, i.e., the interrupting transfer requests will each be handled, then the original, interrupted burst transfer will resume. Col. 6, line 46 to col. 7, line 36.]

19. As per claim 7, Moyer teaches the data processor according to claim 1 wherein said burst transfer suspended is restarted when a certain line related to suspension of said burst transfer is accessed by said processor after said interrupt: [After a burst transfer has been suspended, the bus is used for the interrupting transfer, and later, the suspended burst transfer is resumed. When the suspended burst transfer is resumed, it will transfer a line from memory to the cache (cache burst read). The line transferred is a "certain line related to suspension of said burst transfer" because it is part of data to be transferred in the burst transfer that is interrupted. Col. 6, line 46 to col. 7, line 36.]

20. As per claim 14, Moyer teaches the data processor according to claim 1, further comprising: a register (Control Register 56) to which a predetermined

priority related to an interrupt factor is set, and a judgment unit (Logic Circuit 50) comparing a priority of said interrupt request (Col. 5, lines 21-46) with said predetermined priority set in said register, and judging, from the comparison result, whether said burst transfer is suspended or not. [Col. 4, line 65 to col. 5, line 57 describes the arbitration process, including the comparing of priorities using the Logic Circuit 50 to determine if the current burst transfer is to be interrupted or not.]

21. As per claim 15, Moyer teaches the data processor according to claim 1, further comprising: a register to which permission or non-permission to suspend said burst transfer is set for each interrupt factor, wherein said burst transfer is suspended only when said interrupt request has an interrupt factor that is set so as to permit suspension of said burst transfer. [Control field is a register that holds the permission information. Figs. 5 and 6, col. 6, line 46 to col. 7, line 36.]

22. As per claim 16, Moyer teaches the data processor according to claim 1 wherein said interrupt request is executed after executing an instruction that is already fetched before an interrupt instruction corresponding to said interrupt request is fetched. [The processor executes many instructions prior to executing an interrupt instruction corresponding to said interrupt, which inherently means that many instructions have already been fetched before the interrupt or any corresponding interrupt instructions are executed. Examiner notes that any instructions fetched and executed prior to the interrupt being handled is sufficient to read on the limitations. Fig. 5 demonstrates that the processor performs fetching of instructions through transfers from the memory to cache.]

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 5-6, 8-9, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer, U.S. Patent 6,775,727, in view of Kendall, U.S. Patent 6,836,816.

25. As per claim 5, Moyer teaches the data processor according to claim 2, however fails to teach the data processor further comprising: an information register for keeping information about a point at which said burst transfer is suspended, wherein among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information when said burst transfer is restarted.

26. Kendall teaches a data processor comprising:

f. An information register for keeping information about a point at which a burst transfer is suspended: [Kendal states, "When the interrupting request is finished, the suspended burst transfer can be resumed at block 78 by retrieving the originally requested quadword of data from cache and continuing the transfer with the previously

untransferred words." Kendall further teaches that the data cache is word addressable using the word count control to output bits A0–A1 (fig. 4 and col. 3, lines 44-63). Therefore, it is inherent that information is stored in order to know where the burst left off. Furthermore, the storage location is inherently an information register, since it stores the information.]

g. Wherein among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information when said burst transfer is restarted: [Fig. 7, steps 76-78, and col. 5, lines 4-27.]

27. Kendall teaches that after returning from an interruption of a burst transfer, to continue the burst transfer where it left off instead of starting from the beginning. One of ordinary skill in the art would have recognized that this is advantageous since redundant transfer is not needed, i.e., there is no need to start the burst transfer over at the beginning. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Kendall with those of Moyer to enable the burst transfer to be interrupted without the need to restart the transfer from the beginning upon returning from the interruption.

28. Given the similarities between claim 5 and claims 8 and 12, the arguments as stated for the rejection of claim 5 also apply to claims 8 and 12.

29. As per claim 6, Moyer teaches the data processor according to claim 2 wherein said second storage device has a plurality of lines (Cache 18 has multiple lines, col. 3, lines 10-34), however fails to further teach wherein each line has information about a point at which said burst transfer is suspended and

among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information when said burst transfer is restarted.

30. Kendall teaches a data processor comprising:

h. Storing information about a point at which a burst transfer is suspended: [Kendal states, "When the interrupting request is finished, the suspended burst transfer can be resumed at block 78 by retrieving the originally requested quadword of data from cache and continuing the transfer with the previously untransferred words." Kendall further teaches that the data cache is word addressable using the word count control to output bits A0–A1 (fig. 4 and col. 3, lines 44-63). Therefore, it is inherent that information is stored in order to know where the burst left off. Furthermore, the storage location is inherently an information register, since it stores the information.]

i. Wherein among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information when said burst transfer is restarted: [Fig. 7, steps 76-78, and col. 5, lines 4-27.]

31. Kendall teaches that after returning from an interruption of a burst transfer, to continue the burst transfer where it left off instead of starting from the beginning. One of ordinary skill in the art would have recognized that this is advantageous since redundant transfer is not needed, i.e., there is no need to start the burst transfer over at the beginning. Therefore, it would have been

obvious to one of ordinary skill in the art to combine the teachings of Kendall with those of Moyer to enable the burst transfer to be interrupted without the need to restart the transfer from the beginning upon returning from the interruption.

32. While Moyer, in view of Kendall, teaches to store information regarding the point at which the burst transfer is suspended to allow the burst transfer to continue from where it was interrupted instead of starting the transfer over from the beginning, Moyer, in view of Kendall, fails to teach wherein each line of said second storage stores information about a point at which said burst transfer is suspended.

33. However, Moyer, in view of Kendall, does not specifying where the information is stored, one of ordinary skill in the art would have recognized to store the information regarding the point at which the burst transfer is suspended in each line of the second storage since the second storage is a cache, which is used to stored data and has faster access times than other forms of memory. Furthermore, moving the location of where the information is to be stored to the cache is obvious to one of ordinary skill in the art, since merely moving a location of data is an obvious variation.

34. As per claims 9 and 13, given the similarities between claim 6 and claims 9 and 13, the arguments as stated for the rejection of claim 6 also apply to claims 9 and 13.

35. Claims 10-11 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer, U.S. Patent 6,775,727 in view of Embedded Microprocessor Systems Design, by Kenneth Short, herein referred to as Short.

36. As per claim 10, Moyer teaches the data processor according to claim 1 wherein said burst transfer suspended is restarted when interrupt processing is completed, however, it is not disclosed what causes the interrupting memory access to occur and thus does not teach an explicit interruption of the processor that causes a section of interrupt handling code to be executed (another interpretation of interrupt processing).

37. Short teaches interrupt processing is well known in the art and used by processors to execute system operations among other operations. Short further teaches that interrupts can be maskable and nonmaskable, wherein nonmaskable interrupts cannot be prevented from occurring. Short further teaches interrupts conclude with an EOI command byte which indicates the end of interrupt mode, i.e., the termination of interrupt processing (page 483, last paragraph, pages 491-494, section 14.6, specifically, page 493, last two paragraphs and page 494, first two paragraphs. Adding the nonmaskable interrupts of Short to the system of Moyer would enable a burst transfer that reads data from memory and places it into the cache (see rejection of claim 1) to be interrupted for higher priority operations. Furthermore, Moyer teaches a system where burst transfers are interruptible and resumable.

38. Adding the nonmaskable interrupts to the system of Moyer would cause higher priority interrupts handlers to be executed and enable the interruption of burst transfers. Furthermore, the interrupt handlers for the nonmaskable interrupts of Short include an EOI command, which indicates to terminate interrupt handling. It would have been obvious to one of ordinary skill in the art to

add nonmaskable interrupts to the system of Moyer because, as Short teaches, it allows interruption of events for critical high priority interruptions (478-479).

39. As per claim 11, Moyer, in view of Short, teaches the data processor according to claim 10 wherein when a plurality of interrupt requests occur, a plurality of interrupt processing are executed sequentially and, when an instruction for terminating the last interrupt processing is detected, said burst transfer is restarted. [Short teaches nested interrupts are implemented. Pages 473-474, section 14.4.1 Interrupt Request. After a burst transfer is interrupted, Moyer teaches that it is resumed. Col. 6, lines 45-55.]

40. As per claim 17, Moyer teaches the data processor according to claim 1, however fails to further teach wherein instructions are processed in a pipeline having an instruction fetch stage fetching the instructions, a decode stage decoding the instructions fetched by the instruction fetch stage and an instruction execution stage executing the instructions decoded by the decoded stage, wherein an interrupt process is performed when said interrupt request occurs, and first and second processes are selectively performed in accordance with a priority of said interrupt request as the interrupt process, said first process including a process that said instruction execution stage executing an interrupt instruction corresponding to said interrupt request after executing an instruction that is already fetched before the interrupt instruction is fetched by the instruction fetch stage, and said second process including a process that said instruction stage executing the interrupt instruction before executing an instruction that is

already fetched before the interrupt instruction is fetched by the instruction fetch stage and that is not yet executed by the instruction execution stage.

41. However, Examiner takes Official Notice that implementing processors in a pipeline style is well known in the art and includes fetching, decoding and executing stages.

42. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the processor as a pipelined processor with a fetch, decode and execution stage since Examiner takes Official Notice implementing such a pipelined processor is well known in the art and used to improve instruction processing performed.

43. However, Moyer, in view of the Official Notice taken, fails to teach, wherein an interrupt process is performed when said interrupt request occurs, and first and second processes are selectively performed in accordance with a priority of said interrupt request as the interrupt process, said first process including a process that said instruction execution stage executing an interrupt instruction corresponding to said interrupt request after executing an instruction that is already fetched before the interrupt instruction is fetched by the instruction fetch stage, and said second process including a process that said instruction stage executing the interrupt instruction before executing an instruction that is already fetched before the interrupt instruction is fetched by the instruction fetch stage and that is not yet executed by the instruction execution stage:

44. Short teaches

j. Wherein an interrupt process is performed when said interrupt request occurs, and first and second processes are selectively performed in accordance with a priority of said interrupt request as the interrupt process: [Pages 481-483, Section 14.5.2 and 14.5.3 describes the prioritization of interrupts. Furthermore, Short teaches interrupt processing is well known in the art and used by processors to execute system operations among other operations. Short further teaches that interrupts can be maskable and nonmaskable, wherein nonmaskable interrupts cannot be prevented from occurring (pages 478-479). Adding the nonmaskable interrupts of Short to the system of Moyer would enable a burst transfer that reads data from memory and places it into the cache (see rejection of claim 1) to be interrupted for higher priority operations. Also, Short teaches wherein the prioritized interrupts can be nested, thus a first interrupt would cause a first process to selectively performed and a nested second interrupt would cause a second processor to be selectively performed based on their respective priorities. (Page 473-474, section 14.4.1 and pages 500-501, section 14.9.1)

k. Said first process including a process that said instruction execution stage executing an interrupt instruction corresponding to said interrupt request after executing an instruction that is already fetched before the interrupt instruction is fetched by the instruction fetch stage: [In all conceivable instances there will be at least one instruction that is fetched before the interrupt occurs.]

l. And said second process including a process that said instruction stage executing the interrupt instruction before executing an instruction that is already fetched before the interrupt instruction is fetched by the instruction fetch stage and that is not yet executed by the instruction execution stage: [Short teaches interrupts allow processing of the current instruction to complete before the interrupt instructions are processed. Page 502, paragraph 4.

45. Adding the nonmaskable interrupts to the system of Moyer would cause higher priority interrupts handlers to be executed and be able to interrupt burst transfers. It would have been obvious to one of ordinary skill in the art to add nonmaskable interrupts to the system of Moyer because, as Short states, it allows interruption of events for critical high priority interruptions (478-479).

46. As per claim 18, given the similarities between claim 14 and claim 18, the arguments as stated for the rejection of claim 14 also apply to claim 18.

47. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer, U.S. Patent 6,775,727, in view of Embedded Microprocessor Systems Design, by Kenneth Short, herein referred to as Short and further in view of Kendall, U.S. Patent 6,836,816.

48. As per claim 19, Moyer, teaches a data processor comprising:

m. A processor; [CPU 14, fig. 1.]

n. A first storage device; [System Memory(s) 20, 22 and/or 24 33, fig. 3.]

o. And a second storage device connected between said processor and said first storage device: [Cache 18, fig. 3.]

p. Wherein when a predetermined data required by said processor does not exist in said second storage device, a plurality of data corresponding to one line of said second storage device, including said predetermined data, are read from said first storage device and transferred to a certain line of said second storage device by burst transfer: [Col. 3, lines 10-53.]

q. Moyer teaches where burst transfers can be interrupted and resumed depending on priorities described in the control field (figs. 5 & 6, col. 6, lines 46-55), but does not specifically disclose wherein:

r. And when a first branch instruction is detected during a first burst transfer in the process of executing a first program, said first burst transfer is suspended as a branch target is executed:

s. And said data processor further comprising a register for keeping a first information about a point at which said first burst transfer is suspended, wherein upon completion of execution of said second program, said first burst transfer suspended is restarted based on said first information:

49. Short teaches interrupt processing is well known in the art and used by processors to execute system operations among other operations. Short further teaches that interrupts can be maskable and nonmaskable, wherein nonmaskable interrupts cannot be prevented from occurring (pages 478-479).

Adding the nonmaskable interrupts of Short to the system of Moyer would enable a burst transfer that reads data from memory and places it into the cache (see rejection of claim 1) to be interrupted for higher priority operations. Also, Short teaches wherein the prioritized interrupts can be nested, thus a first interrupt would cause a first process to selectively performed and a nested second interrupt would cause a second processor to be selectively performed based on their respective priorities. (Page 473-474, section 14.4.1 and pages 500-501, section 14.9.1) Lastly, Short teaches wherein an interrupt causes a branch to an Interrupt Service Routine (ISR), which is reached via a branch instruction.

50. Adding the nonmaskable interrupts to the system of Moyer would cause higher priority interrupts handlers to be executed and be able to interrupt burst transfers. It would have been obvious to one of ordinary skill in the art to add nonmaskable interrupts to the system of Moyer because, as Short states, it allows interruption of events for critical high priority interruptions (478-479).

51. However, Moyer, in view of Short, fails to teach said data processor further comprising a register for keeping a first information about a point at which said first burst transfer is suspended, wherein upon completion of execution of said second program, said first burst transfer suspended is restarted based on said first information.

52. However, Kendall teaches a data processor comprising:

t. An information register for keeping information about a point at which a burst transfer is suspended: [Kendal states, "When the interrupting request is finished, the suspended burst transfer can be

resumed at block 78 by retrieving the originally requested quadword of data from cache and continuing the transfer with the previously untransferred words." Kendall further teaches that the data cache is word addressable using the word count control to output bits A0–A1 (fig. 4 and col. 3, lines 44-63). Therefore, it is inherent that information is stored in order to know where the burst left off. Furthermore, the storage location is inherently an information register, since it stores the information.]

u. Wherein upon completion of execution of said second program, said first burst transfer suspended is restarted based on said first information.: [Fig. 7, steps 76-78, and col. 5, lines 4-27.]

53. Kendall teaches that after returning from an interruption of a burst transfer, to continue the burst transfer where it left off instead of starting from the beginning. One of ordinary skill in the art would have recognized that this is advantageous since redundant transfer is not needed, i.e., there is no need to start the burst transfer over at the beginning.

54. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Kendall with those of Moyer to enable the burst transfer to be interrupted without the need to restart the transfer from the beginning upon returning from the interruption.

55. As per claim 20, Moyer, in view of Short and Kendall, teaches the data processor according to claim 19 wherein, when a second branch instruction is detected during a second burst transfer in the process of executing said second program, said second burst transfer is suspended and a third program as a

branch target is executed, said data processor further comprising another register for keeping a second information about a point at which said second burst transfer is suspended, wherein upon completion of execution of said third program, said second burst transfer suspended is restarted based on said second information. [Short teaches nested interrupts, which are prioritized and a second interrupt (branch instruction) will interrupt the first ISR's processing if the second interrupt has a higher priority. (Pages 500-501, section 14.9.1 describes priorities and pages 473-474, section 14.4.1 describes nested interrupts.)

Conclusion

56. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

57. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Baror et al, U.S. Patent 5,438,670. The prior art teaches retrying burst transfers.

Scarpino, U.S. Patent 6,748,496. The prior art teaches interrupting a write burst transfer.

Tsubota, U.S. Patent 6,606,701. The prior art teaches interrupting a burst transfer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KPR

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